July 2010

AR8032 Integrated 10/100 Fast Ethernet Transceiver

General Description

The Atheros AR8032 Fast Ethernet transceiver is a highly integrated physical layer device that transmits and receives high-speed data over standard category 5 (CAT 5) unshielded twisted pair cable.

The AR8032 is compliant with 100 BASE-TX and 10 BASE-T IEEE 802.3 standards. The AR8032 device uses advanced mixed-signal processing technology and integrates functions such as adaptive equalization, and timing recovery to deliver substantial power savings and operation in noisy environments.

The AR8032 device supports the Media Independent Interface (MII) and Reduced Media Independent Interface (RMII) for direct connection to a Fast Ethernet-capable MAC.

The AR8032 supports the Atheros Cable Diagnostic Test (CDT) feature, which uses Time Domain Reflectometry (TDR) technology to quickly and remotely identify potential cable malfunctions without deploying field support personnel or bringing down the network. The AR8032 solution detects and reports issues such as PHY malfunctions, bad/marginal cable or patch cord segments or connectors, thus significantly reducing installation time, cable debug efforts, and overall network support cost.

Manufactured in a standard CMOS process, the AR8032 is packaged in a 32-pin QFN, featuring a small body size of 5 x 5mm.

Features

- 10/100 BASE-T IEEE 802.3 compliant
- Supports MII/RMII interface
- Low power modes with internal automatic DSP power saving scheme
- Fully integrated digital adaptive equalizers All digital baseline wander correction
- Supports external 25 MHz clock source in MII mode
- Supports external 50 MHz clock source in RMII mode
- Automatic speed downshift mode
- Automatic MDI/MDIX crossover
- Automatic polarity correction
- Loopback modes for diagnostics
- IEEE 802.3u compliant Auto-Negotiation
- Software programmable LED modes
- Cable Diagnostic Test (CDT)
- Requires only one 3.3V power supply
- 32-pin QFN 5mm x 5 mm package

AR8032 Functional Block Diagram

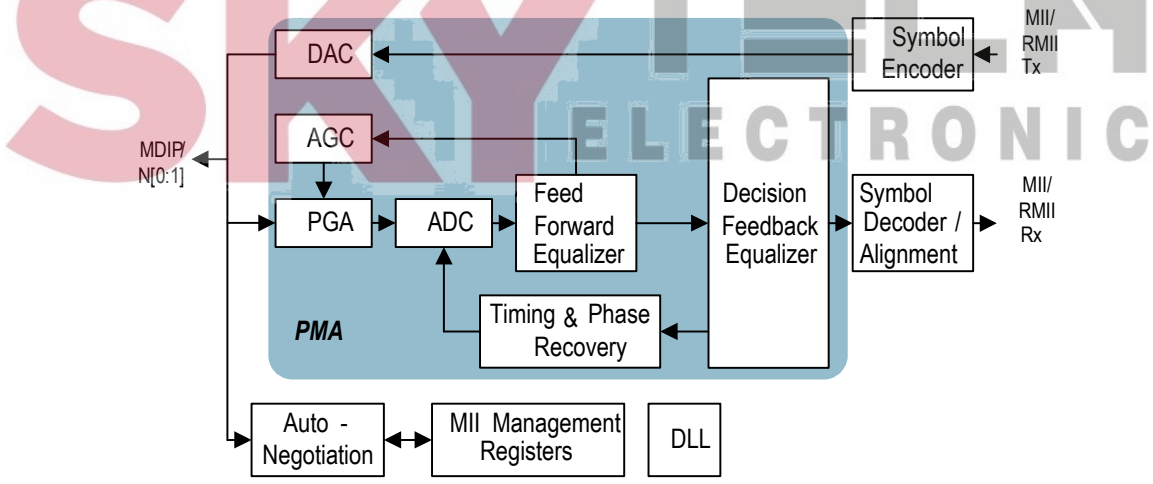

Table of Contents

1. Pin Descriptions

This section contains a package pinout for the AR8032 QFN 32pin and a listing of the signal descriptions (see Figure 1-1).

The following nomenclature is used for signal names:

NC	No connection to the internal die is made from this pin
_#	At the end of the signal name, indicates active low signals
P	Power

The following nomenclature is used for signal types described in Table 1-1:

D	Open drain
IA	Analog input
I	Digital input
IH	Digital input with histeresis
I/O	Digital input/output
OA	Analog output
O	Digital output
PD	Internal pull-down for digital input
PU	Internal pull-up for digital input

Figure 1-1 shows the pinout diagram for the AR8032.

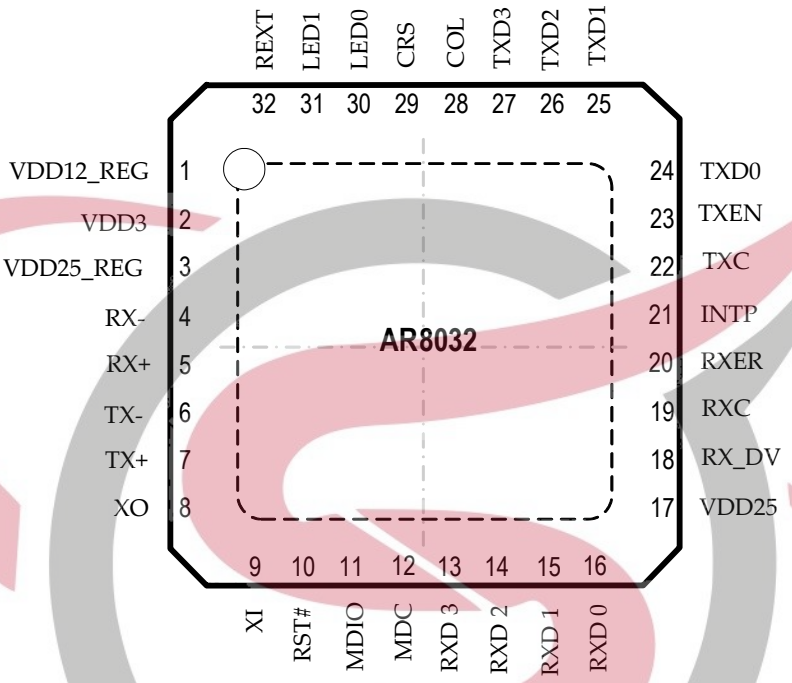

Figure 1-1. **Pinout Diagram**

NOTE: There is an exposed ground pad on the back side of the package.

Table 1-1. **Signal to Pin Relationships and Descriptions**

Symbol	Pin	Type	Description
VDD12_REG	1	AO	1.2V regulator output. A 1 uF plus a 0.1 uF cap needed to stabilize the output
VDD3	2	P	3.3V power supply.
VDD25_REG	3	AO	2.5V regulator output. A 1 uF ceramic cap needed to stabalize the output. It is for analog, digital I/O and the transformer center taps.
RX-	4	AI, AO	Media Dependent Interface 0, terminate with a 49.9Ω resister and connect to XFMR
RX+	5	AI, AO	Media Dependent Interface 0, terminate with a 49.9Ω resister and connect to XFMR
TX-	6	AI, AO	Media Dependent Interface 1, terminate with a 49.9Ω resister and connect to XFMR
TX+	7	AI, AO	Media Dependent Interface 1, terminate with a 49.9Ω resister and connect to XFMR
XO	8	AO	Crystal oscillator output. 27 pF to GND.
XI	9	AI	Crystal oscillator input. 27 pF to GND. An external 25/50 MHx clock source with 1.2V swing can inject from this pin when a crystal is not used and the two 27pF caps removed. The 25 Mhz clock input is for MII mode, while the 50 Mhz clock input is for RMII mode.
RST#	10	IH, PU	System reset input.
MDIO	11	I/O, D, PU	Management data.
MDC	12	I, PU	Management clock reference.
RXD3	13	I/O, PU, POS	MII Receive data output [3].
RXD2	14	I/O, PD, POS	MII Receive data output [2].
RXD1	15	I/O, PD, POS	MII/RMII Receive data output [1].
RXD0	16	I/O, PU, POS	MII/RMII Receive data output [0].
VDD25	17	P	2.5V I/O power, connect with pin 3, 0.1uF to GND.
RX_DV	18	I/O, PD, POS	Receive data valid output
RXC	19	I/O, PD, POS	Receive clock output
RXER	20	I/O, PD, POS	Receive error output
INTP	21	I/O, PU, POS	Interrupt Output
TXC	22	I/O, PU, POS	Transmit clock output
TXEN	23	I, PU	Transmit data enable

Table 1-1. **Signal to Pin Relationships and Descriptions (continued)**

Symbol	Pin	Type	Description
TXD0	24	I, PD	MII/RMII Transmit data input [0]
TXD1	25	I, PD	MII/RMII Transmit data input [1]
TXD2	26	I, PD	MII Transmit data input [2]
TXD3	27	I, PD	MII Transmit data input [3]
COL	28	I/O, PD, POS	Collision Detect output
CRS	29	I/O, PD POS	Carrier Sense output
LED0	30	I/O, PU POS	Programable LED0, the default indicates Link and Activity
LED1	31	I/O, PU POS	Programmable LED1, The default indicates Speed
REXT	32	AO	Connect 2.37 K to GND
PADDLE	GND	Gnd	Ground

NOTE: All of the digital input only pads are 3.3V input tolerant. The O and I/O pads are powered with 2.5V power. The input level of any I/O pads (except open-drain type) is limited to 3 V.

2. Functional Description

The Atheros AR8032 is a highly integrated analog front end (AFE) and digital signal transceiver (see Figure 2-1), providing high performance with substantial cost reduction. AFE consists of automatic gain control (AGC), ADC, DAC, drivers, and clock generation. The AR8032 provides physical layer functions to transmit and receive high-speed data over standard category 5 (CAT5) unshielded twisted pair cable.

See also the "AR8032 Functional Block Diagram" on page 1.

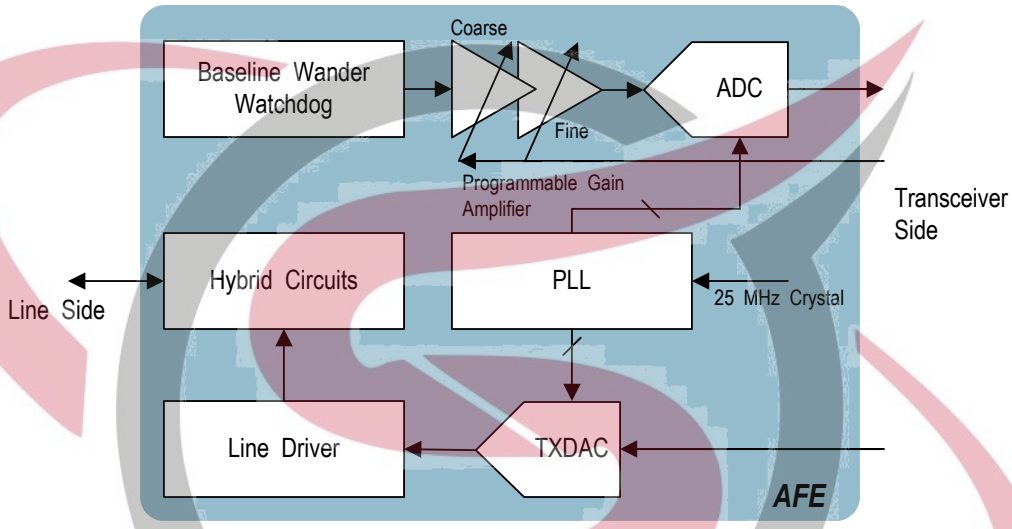

Figure 2-1. **Analog Front End**

The AR8032 10/100 PHY is fully 802.3, 802.3u compliant, and supports the media-independent interface (MII) and Reduced Media Independent Interface (RMII) to connect to a Fast Ethernet-capable MAC.

The AR8032 transceiver combines feed-forward equalizer, feedback equalizer, and timing recovery, to enhance signal performance in noisy environments.

2.1 Transmit Functions

The AR8032 transmit channel includes 4B/5B mapper and scrambler. Table 2-1 describes the transmit function encoder modes.

Table 2-1. **Transmit Function Encoder Modes**

Encoder Mode	Description
100BASE-TX	In 100BASE-TX mode, 4-bit data from the MII is 4B/5B serialized, scrambled, and encoded to a three-level MLT3 sequence transmitted by the PMA.
10BASE-T	In 10BASE-T mode, the AR8032 transmits and receives Manchester-encoded data.

2.2 Receive Functions

The AR8032 receive channel includes digital gain control, feed forward adaptive equalizer, decision feedback equalizer, slicer, 5B/4B de-mapper and de-scrambler, PCS receive functional block, and timing recovery logic.

2.2.1 Decoder Modes

Table 2-2 describes the receive function decoder modes.

Table 2-2. **Receive Function Decoder Modes**

Decoder Mode	Description
100BASE-TX	In 100BASE-TX mode, the receive data stream is recovered and descrambled to align to the symbol boundaries. The aligned data is then parallelized and 5B/4B decoded to 4-bit data. This output runs to the MII/RMII receive data pins after data stream delimiters have been translated.
10BASE-T	In 10BASE-T mode, the recovered 10BASE-T signal is decoded from Manchester then aligned.

2.2.2 Analog to Digital Converter

The AR8032 device employs an advanced high speed ADC on each receive channel with high resolution, which results in better SNR and lower error rates.

2.2.3 Baseline Wander Canceller

Baseline wander results from Ethernet links that AC-couple to the transceivers and from AC coupling that cannot maintain voltage levels for longer than a short time. As a result, transmitted pulses are distorted, resulting in erroneous sampled values for affected pulses. The AR8032 device uses an advanced baseline wander cancellation circuit that continuously monitors and compensates for this effect, minimizing the impact of DC baseline shift on the overall error rate.

2.2.4 Digital Adaptive Equalizer

The digital adaptive equalizer removes inter-symbol interference at the receiver. The digital adaptive equalizer takes unequalized signals from ADC output and uses a combination of feedforward equalizer (FFE) and decision feedback equalizer (DFE) for the best-optimized signal-to-noise (SNR) ratio.

2.2.5 Auto-Negotiation

The AR8032 device supports 10/100 BASE-T Copper auto-negotiation in accordance with IEEE 802.3 clauses 28 and 40. Auto-negotiation provides a mechanism for transferring information between a pair of link partners to choose the best possible mode of operation in terms of speed, duplex modes, and master/slave preference. Auto-negotiation is initiated upon any of the following scenarios:

- Power-up reset
- Hardware reset
- Software reset
- Auto-negotiation restart
- Transition from power-down to power-up
- The link goes down

If auto-negotiation is disabled, a 10BASE-T or 100BASE-TX can be manually selected using the IEEE MII registers.

2.2.6 Smartspeed Function

The Atheros Smartspeed function is an enhanced feature of auto-negotiation that allows the AR8032 device to fall back in speed based on cabling conditions as well as operate over CAT3 cabling (in 10BASE-T mode) or two-pair CAT5 cabling (in 100BASE-TX mode).

By default, the Smartspeed feature is enabled. Refer to the register "Smart Speed Register" on page 38, which describes how to set the parameters. Set these register bits to control the Smartspeed feature:

- Bit [5]: 1 = Enables Smartspeed (default)
- Bits [4:2]: Sets the number of link attempts before adjusting
- Bit [1]: Timer to determine the stable link condition

2.2.7 Polarity Correction

If cabling has been incorrectly wired, the AR8032 automatically corrects polarity errors on the receive pairs.

2.3 Loopback Modes

2.3.1 Digital Loopback

Digital loopback provides the ability to loop transmitted data back to the receiver using digital circuitry in the AR8032 device.

Figure 2-2 shows a block diagram of digital loopback.

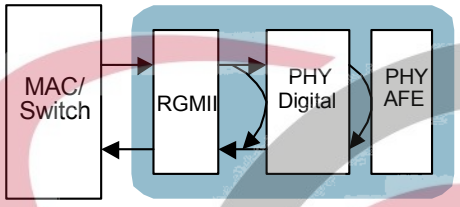

Figure 2-2. **Digital Loopback**

2.3.2 External Cable Loopback

External cable loopback loops MII Tx to MII Rx through a complete digital and analog path and an external cable, thus testing all the digital data paths and all the analog circuits. Figure 2-3 shows a block diagram of external cable loopback.

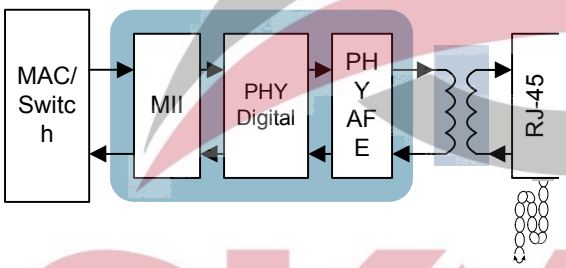

Figure 2-3. **External Cable Loopback**

2.3.3 Cable Diagnostic Test

The Cable Diagnostic Test (CDT) feature in the AR8032 device uses Time Domain Reflectometry (TDR) to identify remote and local PHY malfunctions, bad/marginal cable or patch cord segments, or connectors. Some of the possible problems that can be diagnosed include opens, shorts, cable impedance mismatch, bad connectors, termination mismatch, and bad magnetics. The CDT can be performed when there is no link partner or when the link partner is auto-negotiating.

2.3.4 LED Interface

The LED interface can either be controlled by the PHY or controlled manually, independent of the state of the PHY. Two status LEDs are available. These can be used to indicate operation speed, and link status. The LEDs can be programmed to different status functions from their default value. They can also be controlled directly from the MII register interface.

2.3.5 Power Supplies

The AR8032 device requires only one power supply: 3.3V.

2.3.6 Low Power Modes

The AR8032 device supports the software power-down low power mode. The standard IEEE power-down mode is entered by setting the POWER_DOWN bit (bit [11]) of the register "Control Register" on page 22 equal to one.

In this mode, the AR8032 device ignores all MAC interface signals except the MDC/MDIO. It does not respond to any activity on the CAT 5 cable. The device cannot wake up on its own. It can only wake up by setting the POWER_DOWN bit (bit [11]) of the register "Control Register" on page 22" to 0.

2.3.7 Hibernation Mode

The AR8032 device supports hibernation mode. When the cable is unplugged, the AR8032 will enter hibernation mode after about 10 seconds. The power consumption in this mode is very low compared to the normal mode of operation. When the cable is re-connected, the AR8032 wakes up and normal functioning is restored.

3. Electrical Characteristics

3.1 Absolute Maximum Ratings

Table 3-1 summarizes the absolute maximum ratings and Table 3-2 lists the recommended operating conditions for the AR8032. Absolute maximum ratings are those values beyond which damage to the device can occur. Functional operation under these conditions, or at any other condition beyond those indicated in the operational sections of this document, is not recommended.

Table 3-1. **Absolute Maximum Ratings**

Symbol	Parameter	Max Rating	Unit
VDD33	3.3V supply voltage	3.8	V
T_{store}	Storage temperature	–65 to 150	°C
HBM	Human Body Model	±4500	V
CDM	Charged-Device Model	±1000	V
MM	Machine Model	±200	V

3.2 Recommended Operating Conditions

Table 3-2. **Recommended Operating Conditions**

Symbol	Parameter	Min	Typ	Max	Unit
VDD33	3.3V supply voltage	3.0	3.3	3.6	V
T_A	Ambient Temperature for normal operation — Commercial chip version, AR8032-BL1A (see "Ordering Information — page 53")	0	—	70	°C
	Ambient Temperature for normal operation — Industrial chip version, AR8032-BL1B (see "Ordering Information — page 53")	-40	—	85	°C
T_J	Junction Temperature	-40	—	125	°C
Ψ_{JT}	Thermal Dissipation Coefficient	—	4	—	°C/W

NOTE: The following condition must be satisfied:

$$T_{Jmax} > T_{Cmax} + \Psi_{JT} \times P_{Typical}$$

Where:

T_{Jmax} = Maximum allowable temperature of the Junction

T_{Cmax} = Maximum allowable Case temperature

Ψ_{JT} = Thermal Dissipation Coefficient

$P_{Typical}$ = Typical power dissipation

3.3 XTAL/OSC Timing

Figure 3-1 shows the XTAL timing diagram.

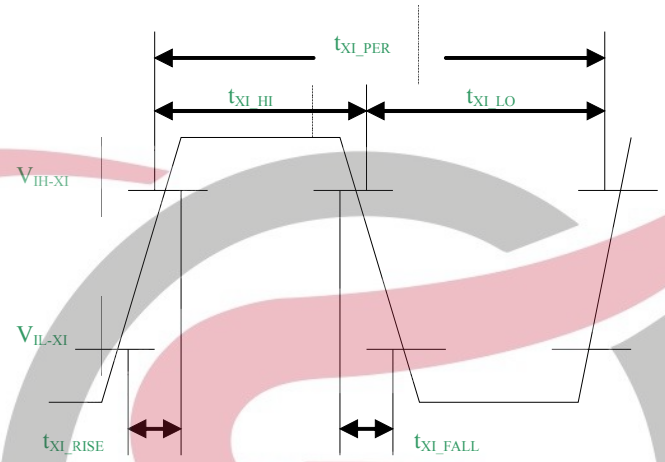

Figure 3-1. **XTAL/OSC Timing Diagram**

Table 3-3. **XTAL/OSC Timing — MII mode**

Symbol	Parameter	Min	Typ	Max	Unit
T_XI_PER	XI/OSCI Clock Period	40.0 - 50ppm	40.0	40.0 + 50ppm	ns
T_XI_HI	XI/OSCI Clock High	14	20.0		ns
T_XI_LO	XI/OSCI Clock Low	14	20.0		ns
T_XI_RISE	XI/OSCI Clock Rise Time, V_{IL} (max) to V_{IH} (min)			4	ns
T_XI_FALL	XI/OSCI Clock Fall time, V_{IL} (max) to V_{IH} (min)			4	ns
V_IH_XI	The XTLI input high level	0.8	1.2	1.5	V
V_IL_XI	The xtli input low lever voltage	-0.3	0	0.15	V

Table 3-4. **XTAL/OSC Timing — RMII mode**

Symbol	Parameter	Min	Typ	Max	Unit
T_XI_PER	XI/OSCI Clock Period	20.0 - 50ppm	20.0	20.0 + 50ppm	ns
T_XI_HI	XI/OSCI Clock High	8	10.0		ns
T_XI_LO	XI/OSCI Clock Low	8	10.0		ns

T_XI_RISE	XI/OSCI Clock Rise Time, V_{IL} (max) to V_{IH} (min)			2	ns
T_XI_FALL	XI/OSCI Clock Fall time, V_{IL} (max) to V_{IH} (min)			2	ns
V_IH_XI	The XTLI input high level	0.8	1.2	1.5	V
V_IL_XI	The xtli input low level voltage	-0.3	0	0.15	V

3.4 MII DC Characteristics

Table 3-5 shows the MII DC characteristics.

Table 3-5. **MII DC Characteristics**

Symbol	Parameter	Min	Max	Unit
V_{OH}	Output high voltage	2.4	3.0	V
V_{OL}	Output low voltage	GND	0.4	V
V_{IH}	Input high voltage	1.7	—	V
V_{IL}	Input low voltage	—	0.7	V
I_{IH}	Input high current	—	15	µA
I_{IL}	Input low current	–15	—	µA

Figure 3-2 shows the MII input AC timing diagram.

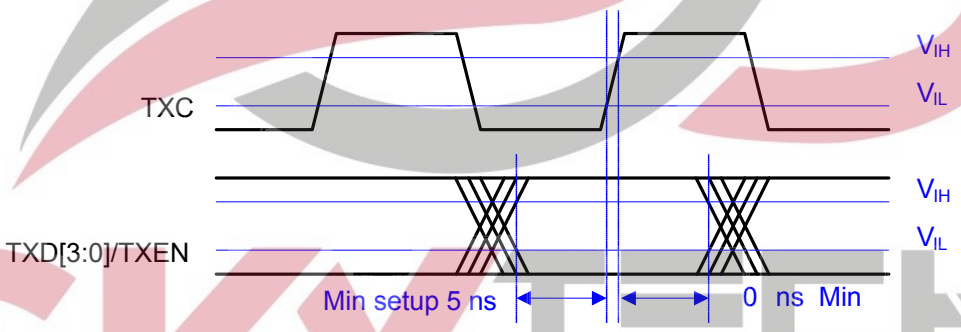

Figure 3-2. **MII Input AC Timing Diagram**

Figure 3-3 shows the MII output AC timing diagram.

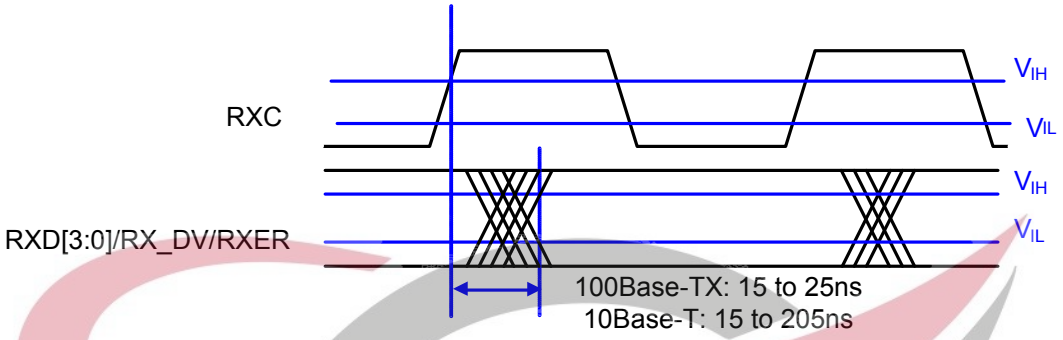

Figure 3-3. **MII Output AC Timing Diagram**

3.5 MDIO Characteristics

Table 3-6 shows the MDIO DC characteristics.RMII Timing

Table 3-6. **MDIO DC Characteristics**

Symbol	Parameter	Min	Max	Unit
V_{OH}	Output high voltage	2.4	—	V
V_{OL}	Output low voltage	—	0.4	V
V_{IH}	Input high voltage	2	—	V
V_{IL}	Input low voltage	—	0.8	V
I_{IH}	Input high current	—	0.4	mA
I_{IL}	Input low current	-0.4	—	mA

3.5.8 MDIO Timing

Figure 3-4 shows the MDIO timing diagram.

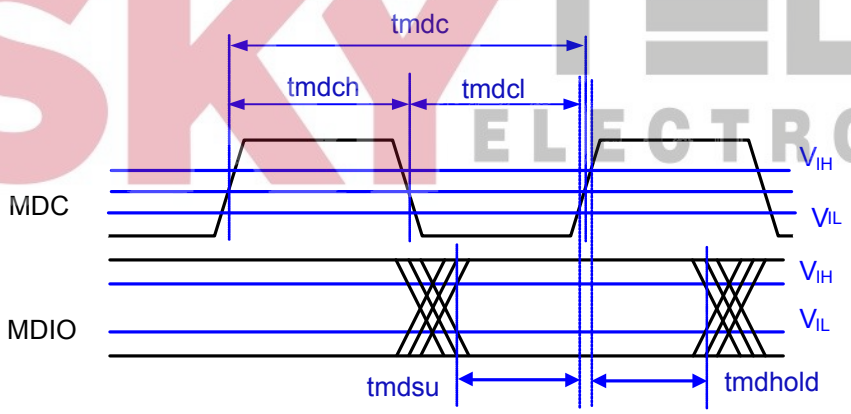

Figure 3-4. **MDIO Timing Diagram**

Table 3-7 shows the RMII AC timing characteristics.

Table 3-7. **MDIO Timing**

Symbol	Parameter	Min	Typ	Max	Unit
tmdc	MDC Period	100			nS
tmdcl	MDC Low Period	40			nS
tmdch	MDC High Period	40			nS
tmdsu	MDIO to MDC rising setup time	10			nS
tmdhold	MDIO to MDC rising hold time	10			nS

Table 3-8 shows the RMII AC timing characteristics.

Table 3-8. **RMII AC Timing**

Symbol	Parameter	Min	Max	Unit
Tck	XI Period	20 -50ppm	20 +50ppm	nS
Tsu	TXEN, TXD to XI rising setup time	4	—	nS
Thold	TXEN, TXD to XI rising hold time	2	—	nS
Tdly	XI to RX_DV, RXD output delay	3	14	nS

Figure 3-5 shows the AC RMII timing diagram.

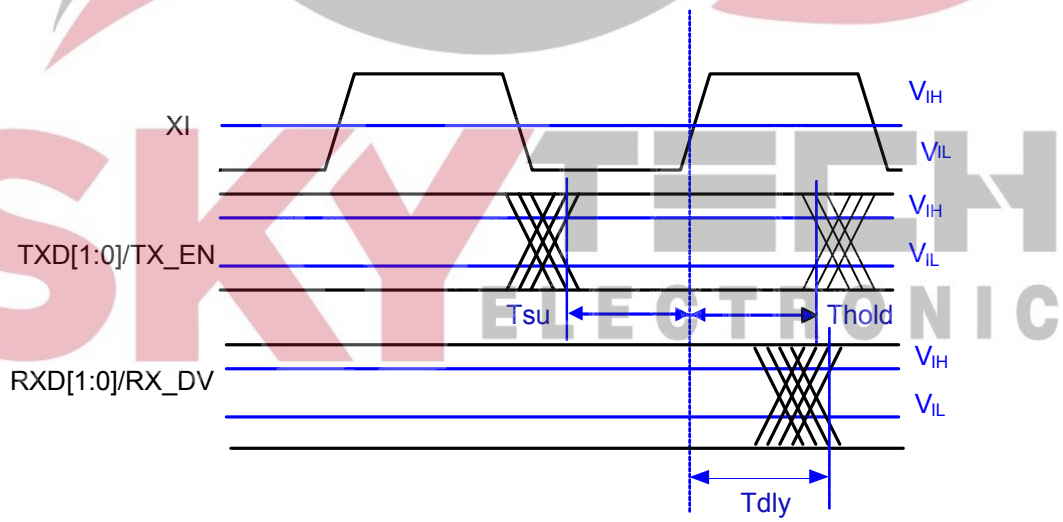

Figure 3-5. **RMII AC Timing Diagram**

3.6 Power-On Strapping

Table 3-9 shows the pin-to-PHY core configuration signal power-on strapping.

Table 3-9. **Power-On Strapping[1]**

PHY Pin Name	Pin	PHY Core Configuration Signal	Description		Default
RXD3	13	PHYADDRESS[0]	RXD[1:3] set the lower three bits of the physical address. The upper two bits of the physical address default to 001		1
RXD2	14	PHYADDRESS[1]			0
RXD1	15	PHYADDRESS[2]			0
RXD0	16	DUPLEX	0	Half Duplex	1
			1	Full Duplex	
RXDV	18	CONFIG2	CONFIG[2:0] 000 = MII 001 = RMII All other binary combinations are Reserved.		000
CRS	29	CONFIG1			
COL	28	CONFIG0			
RXER	20	ISOLATE	0	Disable	0
			1	Enable	
INTP	21	TEST MODE	0	Test Mode	1
			1	Normal Operation	
LED0	30	AUTO-NEGOTIATION	0	Disable	1
			1	Enable	
LED1	31	SPEED	0	10Base-T	1
			1	100Base-Tx	
RXC	19	POWER DOWN MODE	0	Disable	0
			1	Enable	
TXC	22	Reserved			1

[1]Default values: 0 = Pull-down, 1 = Pull-up with 10 K resistor.

3.7 Typical Power Consumption Parameters

The following conditions apply to the typical characteristics unless otherwise specified:

V_{DD33} = 3.3V, T_{amb} = 25 °C

Table 3-10 shows the typical power drain as a function of the AR8032's operating mode.

Table 3-10. **Total System Power**

Symbol	AR8032 Power Consumption (mW)	Total System (includes XFMR and LED0 Power Consumption (mW)	Description
P_{LDPS}	10.9	10.9	Link down, power-saving mode
P_{PWD}	6.6	6.6	Power Down Mode

Table 3-10. **Total System Power**

Symbol	AR8032 Power Consumption (mW)	Total System (includes XFMR and LED0 Power Consumption (mW)	Description
$P_{Isolate}$	39.6	52.8	Isolate mode
P_{100F}	123	280	100Base-T Full Duplex
P_{10F}	52.5	272	10Base-T Full Duplex
P_{10TX}	49.5	257.4	10Base-T Transmit
P_{10RX}	49.5	59.4	10Base-T Receive
P_{10IDLE}	47.8	69.3	10Base-T Idle

NOTE: Total power includes power consumed by the center-tap of the transformer and the LEDs

Table 3-11 shows the Power Output Parameters of the AR8032's operating mode.

Table 3-11. **Power Output Parameters**

Symbol	Voltage Range	Total Consumption
VDD12_REG	1.2V ±5%	34 mA
VDD25_REG	2.5V +10%/-5%	70 mA

NOTE: The 1.2V only has one regulator outpur pin, so the 1.2V current does not appear on the board. The VDD25_REG total comsumption includes center tap power consumption.

3.8 Power-on Sequence, Reset and Clock

3.8.1 Power-on Sequence

The AR8032 only needs a single 3.3V power supply input. The 1.2V core and 2.5V I/O voltages are generated by AR8032's internal LDOs. So the AR8032's power-on sequence to establish the power rails stability is met internally.

3.8.2 Reset and Clock Timing

Figure 3-6 shows the Power-on Timing diagram.

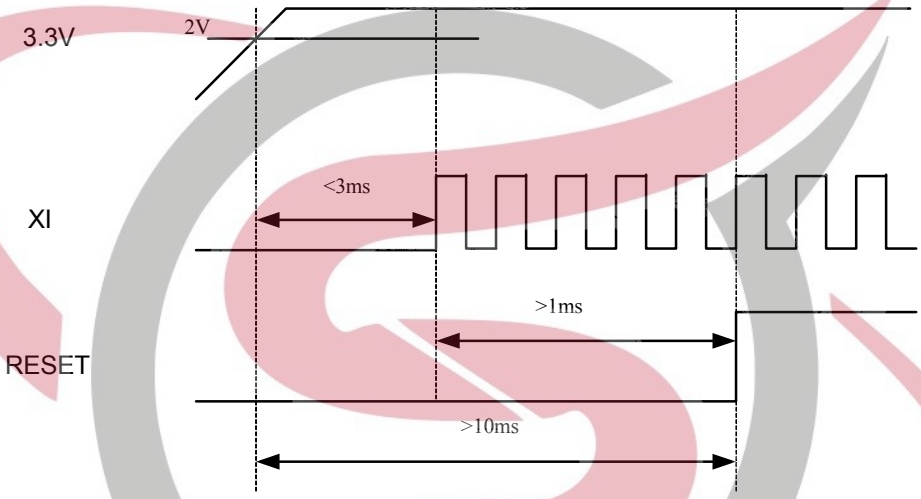

Figure 3-6. **Power-on Timing Diagram**

AR8032 provides a hardware RESET pin, which must be asserted during power on and kept low for at least 10 ms after 3.3V rail reaches 2V.

AR8032 clock input XI must be supplied within 3ms after 3.3V rail reaching 2V and must be kept stable for at least 1ms before RESET is brought to high.

If designs with an external 25MHz clock (for MII mode) or 50MHz (for RMII mode) can not meet the 3.3v to XI within the 3ms requirement, the PHY registers need be initialized (different from default value) immediately, as in the following — write debug register 0x12[3]=1'b0 then write debug register 0x29[2:0]=3'b100.

Once the power 3.3V rail is stable and clock XI is present then subsequent hardware reset signal must be a minimum of 1ms in duration.

Figure 3-7 shows the Warm Hardware Reset Diagram.

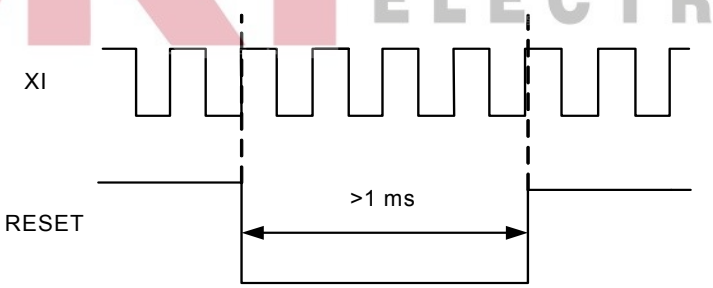

Figure 3-7. **Warm Hardware Reset Diagram**

4. Register Descriptions

Table 4-1 shows the reset types used in this document.

Table 4-1. **Reset Types**

Type	Description
LH	Register field with latching high function. If status is high, then the register is set to one and remains set until a read operation is performed through the management interface or a reset occurs.
LL	Register field with latching low function. If status is low, then the register is cleared to a zero and remains cleared until a read operation is performed through the management interface or a reset occurs.
Retain	Value written to a register field takes effect without a software reset.
SC	Self-Clear. Writing a one to this register causes the desired function to execute immediately, and the register field clears to zero when the function is complete.
Update	The value written to the register field does not take effect until a software reset is executed. The value can still be read after it is written.
RES	Reserved for future use. All reserved bits are read as a zero unless otherworse noted.
RO	Read Only
ROC	Read Only Clear. After read, register field is cleard to zero.

Table 4-1. **Reset Types (continued)**

Type	Description
R/W	Read/Write
RWC	Read/Write Clear. After read, register field is cleared to zero.
RWR	Read/Write Reset. All bits are readable and writable. After reset or read, the register field is cleard to zero.
RWS	Read/Write Set. All bits are readable and writable. After reset or read, the register field is set to a non-zero value specified in the text.
SC	Self-Clear. Writing a one to this register causes the desired function to be immediately executed, then the register field is cleared to zero when the function is complete.
WO	Write Only. Reads to this type of register return undefined data.

4.1 PHY Register Summary

Table 4-2 summarizes the registers for the AR8032.

Table 4-2. **Register Summary**

Offset	Register	Page
0x00	Control Register	page 22
0x01	Status	page 24
0x02	PHY Identifier	page 26
0x03	PHY Identifier 2	page 26
0x04	Auto-Negotiation Advertisement	page 29
0x05	Link Partner Ability	page 30
0x06	Auto-Negotiation Expansion	page 29
0x07	Reserved	
0x08	Reserved	
0x09	Reserved	
0x0A	Reserved	
0x0B	Reserved	

Table 4-2. **Register Summary (continued)**

Offset	Register	Page
0x0C	Reserved	
0x0D	Reserved	
0x0E	Reserved	
0x0F	Reserved	
0x10	Function Control Register	page 22
0x11	PHY Specific Status Register	page 33
0x12	Interrupt Enable Register	page 34
0x13	Interrupt Status Register	page 36
0x14	Smart Speed Register	page 38
0x15	Recieve Error Counter Register	page 40
0x16	Virtual Cable Tester Control Register	page 40
0x18	LED Control Register	page 41
0x19	Reserved	
0x1A	Reserved	
0x1B	Reserved	
0x1C	Virtual Cable Tester Status Register	page 40
0x1D	Debug Port (Address Offset Set)	page 43
0x1E	Debug Port 2 (R/W Port) Register	page 43
0x1F	Reserved	
	Debug Register	
0x12	10 Base-T Test Configuration Register	page 44
0x10	100 Base-TX Test Configuration Register	page 45
0x0B	Hibernate Control Register	page 47
0x29	Power Saving Control	page 48

4.1.1 Control Register

Offset: 0x00

Bit	Name	Type		Description
15	Reset	Mode	R/W	PHY Software Reset. Writing a "1" to this bit causes the PHY the reset operation is done , this bit is cleared to "0" automatically. The reset occurs immediately. 1= PHY reset 0 =Normal operation
		HW Rst	0	
		SW Rst	SC	
14	Loopback	Mode	R/W	When loopback is activated, the transmitter data presented on TXD is looped back to RXD internally. Link is broken when loopback is enabled. 1 = Enable Loopback 0 = Disable Loopback
		HW Rst	0	
		SW Rst	0	

Bit	Name	Type		Description
13	Speed Selection (LSB)	Mode	R/W	Upon hardware reset , this bit and 0.6 bit depend upon anen(bit0.12) and SPEED: anen {0.6 , 0.13} 0 {0, SPEED} 1 2'b01 (00:10Mbps, 01:100Mbps, 10:Reserved, 11:Reserved)
		HW Rst	See Desc.	
		SW Rst	Retain	
12	Auto-negotiation	Mode	R/W	Upon hardware reset, this bit depends on ANEN_PAD. 1 = Enable Auto-Negotiation Process 0 = Disable Auto-Negotiation Process
		HW Rst	See Desc.	
		SW Rst	Retain	
11	Power Down	Mode	R/W	When the port is switched from power down to normal operation, software reset and restart Auto-Negotiation are performed even when bits Reset (0.15) and Restart Auto-Negotiation (0.9) are not set by the user. 1 = Power down 0 = Normal operation
		HW Rst	0	
		SW Rst	0	
10	Isolate	Mode	R/W	The MII output pins are tristated when this bit is set to 1. The MII inputs are ignored. 1 = Isolate 0 = Normal operation
		HW Rst	0	
		SW Rst	0	
9	Restart Auto-negotiation	Mode	R/W, SC	Auto-Negotiation automatically restarts after hardware or software reset regardless of whether or not the restart bit (0.9) is set. 1 = Restart Auto-Negotiation Process 0 = Normal operation
		HW Rst	0	
		SW Rst	SC	
8	Duplex mode	Mode	R/W, SC	Upon hardware reset, this bit bit depends on DUPLEX_MODE_PAD and anen bit(0.12): 0.12 0.8 0 0 1 DUPLEX_MODE_PAD 1:Full Duplex 0:Half Duplex
		HW Rst	See Desc.	
		SW Rst		
7	Collision Test	Mode	R/W	Setting this bit to 1 will cause the COL pin to assert whenever the TX_EN pin is asserted. 1 = Enable COL signal test 0 = Disable COL signal test
		HW Rst	0	
		SW Rst	0	
6	Speed Selection (MSB)	Mode	R/W	See bit 0.13.
		HW Rst	See Desc.	
		SW Rst		

Bit	Name	Type		Description
5:0	RES	Mode	RO	Reserved for future use.
		HW Rst	00000	
		SW Rst	00000	

4.1.2 Status Register

Offset: 0x01

Bit	Name	Type		Description
15	100Base-T4	Mode	RO	100BASE-T4. This protocol is not available. 0 = PHY not able to perform 100BASE-T4
		HW Rst	0	
		SW Rst	0	
14	100Base-Tx Full-Duplex	Mode	RO	Capable of 100Base-Tx Full-Duplex operation
		HW Rst	1	
		SW Rst	1	
13	100Base-Tx Half-Duplex	Mode	RO	Capable of 100Base-Tx Half-Duplex operation
		HW Rst	1	
		SW Rst	1	
12	10 Mbps Full-Duplex	Mode	RO	Capable of 10Base-T Full-Duplex operation
		HW Rst	1	
		SW Rst	1	
11	10 Mbps Half-Duplex	Mode	R/W	Capable of 10 Mbps Half-Duplex operation
		HW Rst	1	
		SW Rst	1	
10	100Base-T2 Full-Duplex	Mode	RO	Not able to perform 100Base-T2 Full-Duplex operation
		HW Rst	0	
		SW Rst	0	

Bit	Name	Type		Description
9	100Base-T2 Half-Duplex	Mode	R/W	Not able to perform 100Base-T2 Half-Duplex operation
		HW Rst	0	
		SW Rst	0	
8	Extended Status	Mode	RO	Extended status information in register 15
		HW Rst	1	
		SW Rst	1	
7	RES	Mode	RO	Reserved
		HW Rst	0	
		SW Rst	0	
6	MF Preamble Suppression	Mode	RO	PHY accepts management frames with preamble suppressed
		HW Rst	1	
		SW Rst	1	
5	Auto-negotiation Complete	Mode	RO	1: Auto negotiation process complete 0:Auto negotiation process not complete
		HW Rst	0	
		SW Rst	0	
4	Remote Fault	Mode	RO, LH	1: Remote fault condition detected 0:Remote fault condition not detected
		HW Rst	0	
		SW Rst	0	
3	Auto-Negotiation Ability	Mode	R/W	1: PHY able to perform auto-negotiation
		HW Rst	1	
		SW Rst	1	
2	Link Status	Mode	RO, LL	This register bit indicates whether the link was lost since the last read. For the current link status, read register bit 17.10 Link Real Time. 1 = Link is up 0 = Link is down
		HW Rst	0	
		SW Rst	0	

Bit	Name	Type		Description
1	Jabber Detect	Mode	RO, LH	1: Jabber condition detected 0: Jabber condition not detected
		HW Rst	0	
		SW Rst	0	
0	Extended Capability	Mode	RO	1: Extended register capabilitites
		HW Rst	1	
		SW Rst	1	

4.1.3 PHY Identifier

Offset: 0x02

Bit	Name	Type		Description
15:0	Organizationally Unique Identifer Bits 3:18	Mode	RO	Organizationally Unique Identifer Bits 3:18
		HW Rst	Always 16'h 004d	
		SW Rst	Always 16'h 004d	

4.1.4 PHY Identifier 2

Offset: 0x03

Bit	Name	Type		Description
15:0	OUI bit 19:24 Model Number Revision Number	Mode	RO	
		HW Rst	Always 16'h d023	
		SW Rst	Always 16'h d023	

4.1.5 Auto-Negotiation Advertisement Register

Offset: 0x04

Bit	Name	Type		Description
15	Next Page	Mode	R/W	The value of this bit will be updated immediately after writing this register. But the value written to this bit does not takes effect until any one of the following occurs: o Software reset is asserted (register 0.15) o Restart Auto-Negotiation is asserted (register 0.9) o Power down (register 0.11) transitions from power down to normal operation o Link goes down If 1000BASE-T is advertised then the required next pages are automatically transmitted. Register 4.15 should be set to 0 if no additional next pages are needed. 1 = Advertise 0 = Not advertised
		HW Rst	0	
		SW Rst	Update	
14	Ack	Mode	RO	Must be 0
		HW Rst	Always 0	
		SW Rst	Always 0	
13	Remote Fault	Mode	R/W	1 = Set Remote Fault bit 0 = Do not set Remote Fault bit
		HW Rst	See Desc.	
		SW Rst	Update	
12	Reserved	Mode	RO	Always 0.
		HW Rst	Always 0	
		SW Rst	Always 0	
11	Asymmetric Pause	Mode	R/W	Upon hardware reset , this bit depends on ASYM_PAUSE_PAD. The value of this bit will be updated immediately after writing this register. But the value written to this bit does not takes effect until any one of the following occurs: o Software reset is asserted (register 0.15) o Restart Auto-Negotiation is asserted (register 0.9) o Power down (register 0.11) transitions from power down to normal operation o Link goes down 1 = Asymmetric Pause 0 = No asymmetric Pause
		HW Rst	See Desc.	
		SW Rst	Update	

Bit	Name	Type		Description
10	PAUSE	Mode	R/W	Upon hardware reset , this bit depends on PAUSE_PAD. The value of this bit will be updated immediately after writing this register. But the value written to this bit does not takes effect until any one of the following occurs: o Software reset is asserted (register 0.15) o Restart Auto-Negotiation is asserted (register 0.9) o Power down (register 0.11) transitions from power down to normal operation o Link goes down 1 = MAC PAUSE implemented 0 = MAC PAUSE not implemented
		HW Rst	See Desc.	
		SW Rst	Update	
9	100BASE-T4	Mode	RO	Not able to perform 100BASE-T4
		HW Rst	Always 0	
		SW Rst	Always 0	
8	100BASE-TX Full Duplex	Mode	R/W	The value of this bit will be updated immediately after writing this register. But the value written to this bit does not takes effect until any one of the following occurs: o Software reset is asserted (register 0.15) o Restart Auto-Negotiation is asserted (register 0.9) o Power down (register 0.11) transitions from power down to normal operation o Link goes down 1 = Advertise 0 = Not advertised
		HW Rst	1	
		SW Rst	Update	
7	100BASE-TX Half Duplex	Mode	R/W	The value of this bit will be updated immediately after writing this register. But the value written to this bit does not takes effect until any one of the following occurs: o Software reset is asserted (register 0.15) o Restart Auto-Negotiation is asserted (register 0.9) o Power down (register 0.11) transitions from power down to normal operation o Link goes down 1 = Advertise 0 = Not advertised
		HW Rst	1	
		SW Rst	Update	
6	10BASE-TX Full Duplex	Mode	R/W	The value of this bit will be updated immediately after writing this register. But the value written to this bit does not takes effect until any one of the following occurs: o Software reset is asserted (register 0.15) o Restart Auto-Negotiation is asserted (register 0.9) o Power down (register 0.11) transitions from power down to normal operation o Link goes down 1 = Advertise 0 = Not advertised
		HW Rst	1	
		SW Rst	Update	

Bit	Name	Type		Description
5	10BASE-TX Half Duplex	Mode	R/W	The value of this bit will be updated immediately after writing this register. But the value written to this bit does not takes effect until any one of the following occurs: o Software reset is asserted (register 0.15) o Restart Auto-Negotiation is asserted (register 0.9) o Power down (register 0.11) transitions from power down to normal operation o Link goes down 1 = Advertise 0 = Not advertised
		HW Rst	1	
		SW Rst	Update	
4:0	Selector field	Mode	RO	Selector Field mode 00001 = 802.3
		HW Rst	Always 00001	
		SW Rst	Always 00001	

4.1.6 *Auto-Negotiation Expansion Register*

Offset: 0x06

Bit	Name	Type		Description
15:5	RES	Mode	RO	Reserved. Must be 0.
		HW Rst	Always 0	
		SW Rst	Always 0	
4	Parallel Detection Fault	Mode	RO, LH	1: a fault has been detect 0: no fault has been detected
		HW Rst	0	
		SW Rst	0	
3	Link Partner Next Page Able	Mode	RO	1: Link partner is Next page able 0: Link partner is not next page able
		HW Rst	0	
		SW Rst	0	
2	Local Next Page Able	Mode	RO	1: Local Device is Next Page able 0: Local Device is not Next Page able
		HW Rst	0	
		SW Rst	0	

Bit	Name	Type		Description
1	Page Received	Mode	RO, LH	1: A new page has been received 0: No new page has been received
		HW Rst	0	
		SW Rst	0	
0	Link Partner Auto-Negotiation Able	Mode	RO	1: Link partner is auto negotiation able 0: Link partner is not auto negotiation able
		HW Rst	0	
		SW Rst	0	

4.1.7 *Link partner ability register(base page)*

Offset: 0x05

Bit	Name	Type		Description
15	Next page	Mode	RO	Received Code Word Bit 15 1 = Link partner capable of next page 0 = Link partner not capable of next page
		HW Rst	0	
		SW Rst	0	
14	Ack	Mode	RO	Acknowledge Received Code Word Bit 14 1 = Link partner received link code word 0 = Link partner does not have Next Page ability
		HW Rst	0	
		SW Rst	0	
13	Remote Fault	Mode	RO	Remote Fault Received Code Word Bit 13 1 = Link partner detected remote fault 0 = Link partner has not detected remote fault
		HW Rst	0	
		SW Rst	0	
12	Reserved	Mode	RO	Technology Ability Field Received Code Word Bit 12
		HW Rst	0	
		SW Rst	0	
11	Asymmetric Pause	Mode	RO	Technology Ability Field Received Code Word Bit 11 1 = Link partner requests asymmetric pause 0 = Link partner does not request asymmetric pause
		HW Rst	0	
		SW Rst	0	

Bit	Name	Type		Description
10	PAUSE	Mode	RO	Technology Ability Field Received Code Word Bit 10 1 = Link partner is capable of pause operation 0 = Link partner is not capable of pause operation
		HW Rst	0	
		SW Rst	0	
9	100BASE-T4	Mode	RO	Technology Ability Field Received Code Word Bit 9 1 = Link partner is 100BASE-T4 capable 0 = Link partner is not 100BASE-T4 capable
		HW Rst	0	
		SW Rst	0	
8	100BASE-TX Full Duplex	Mode	RO	Technology Ability Field Received Code Word Bit 8 1 = Link partner is 100BASE-TX full-duplex capable 0 = Link partner is not 100BASE-TX full-duplex capable
		HW Rst	0	
		SW Rst	0	
7	100BASE-TX Half Duplex	Mode	RO	Technology Ability Field Received Code Word Bit 7 1 = Link partner is 100BASE-TX half-duplex capable 0 = Link partner is not 100BASE-TX half-duplex capable
		HW Rst	0	
		SW Rst	0	
6	10BASE-TX Full Duplex	Mode	RO	Technology Ability Field Received Code Word Bit 6 1 = Link partner is 10BASE-T full-duplex capable 0 = Link partner is not 10BASE-T full-duplex capable
		HW Rst	0	
		SW Rst	0	
5	10BASE-TX Half Duplex	Mode	RO	Technology Ability Field Received Code Word Bit 5 1 = Link partner is 10BASE-T half-duplex capable 0 = Link partner is not 10BASE-T half-duplex capable
		HW Rst	0	
		SW Rst	0	
4:0	Selector field	Mode	RO, LH	Selector Field Received Code Word Bit 4:0
		HW Rst	0	
		SW Rst	0	

4.1.8 Function Control Register

Offset: 0x10

Bit	Name	Type		Description
15:12	RES	Mode	R/W	Reserved
		HW Rst	0	
		SW Rst	Retain	
11	Assert CRS on Transmit	Mode	R/W	1 = when transmitting, crs_o is asserted to 1; 0 = crs_o is asserted to 1 only when receiving. When in RMII mode, this bit is fixed to 0.
		HW Rst	1	
		SW Rst	Retain	
10	RES	Mode	R/W	Reserved
		HW Rst	0	
		SW Rst	Retain	
9:7	RES	Mode	R/W	Reserved
		HW Rst	0	
		SW Rst	Retain	
6:5	MDI Crossover Mode	Mode	R/W	Changes to these bits are disruptive to the normal operation; therefore any changes to these registers must be followed by a software reset to take effect. 00 = Manual MDI configuration 01 = Manual MDIX configuration 10 = Reserved 11 = Enable automatic crossover for all modes
		HW Rst	11	
		SW Rst	Update	
4:3	RES	Mode	R/W	Reserved
		HW Rst	0	
		SW Rst	Retain	
2	SQE Test	Mode	R/W	SQE Test is automatically disabled in full-duplex mode 1 = SQE test enabled 0 = SQE test disabled
		HW Rst	0	
		SW Rst	Retain	
1	RES	Mode	R/W	Reserved
		HW Rst	1	
		SW Rst	Retain	

Bit	Name	Type		Description
0	Disable Jabber	Mode	R/W	Jabber has effect only in 10BASE-T half-duplex mode. 1 = Disable jabber function 0 = Enable jabber function
		HW Rst	0	
		SW Rst	Retain	

4.1.9 PHY Specific Status Register

Offset: 0x11

Bit	Name	Type		Description
15:14	Speed	Mode	RO	These status bits are valid only after resolved bit 17.11 = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. 11 = Reserved 10 = Reserved 01 = 100 Mbps 00 = 10 Mbps
		HW Rst	00	
		SW Rst	Retain	
13	Duplex	Mode	RO	This status bit is valid only after resolved bit 17.11 = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. 1 = Full-duplex 0 = Half-duplex
		HW Rst		
		SW Rst		
12	Page Received (real-time)	Mode	RO	1 = Page received 0 = Page not received
		HW Rst	0	
		SW Rst	Retain	
11	Speed and Duplex Resolved	Mode	RO	When Auto-Negotiation is not enabled, 17.11 = 1 for force speed mode. 1 = Resolved 0 = Not resolved
		HW Rst	0	
		SW Rst	0	
10	Link (real-time)	Mode	RO	1 = Link up 0 = Link down
		HW Rst	0	
		SW Rst	0	
9:7	RES	Mode	RO	Reserved
		HW Rst	Always 0	
		SW Rst	Always 0	

Bit	Name	Type		Description
6	MDI Crossover Status	Mode	RO	This status bit is valid only after resolved bit 17.11 = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. This bit is 0 or 1 depending on what is written to 16.6:5 in manual configuration mode. Register 16.6:5 are updated with software reset. 1 = MDIX 0 = MDI
		HW Rst	0	
		SW Rst	Retain	
5	Wirespeed Downgrade	Mode	RO	1 = Downgrade 0 = No Downgrade
		HW Rst	0	
		SW Rst	0	
4	RES	Mode	RO	Reserved
		HW Rst	1	
		SW Rst	1	
3	Transmit Pause Enabled	Mode	RO	This is a reflection of the MAC pause resolution. This bit is for information purposes and is not used by the device. This status bit is valid only after resolved bit 17.11 = 1. The resolved bit is set when Auto-Negotiation is completed; While in force mode, this bit is set to be 0. 1 = Transmit pause enabled 0 = Transmit pause disabled
		HW Rst		
		SW Rst		
2	Receive Pause Enabled	Mode	RO	This is a reflection of the MAC pause resolution. This bit is for information purposes and is not used by the device. This status bit is valid only after resolved bit 17.11 = 1. The resolved bit is set when Auto-Negotiation is completed; While in force mode, this bit is set to be 0. 1 = Receive pause enabled 0 = Receive pause disabled
		HW Rst		
		SW Rst		
1	Polarity (real-time)	Mode	RO	1 = Reversed 0 = Normal
		HW Rst	0	
		SW Rst	Retain	
0	Jabber (real-time)	Mode	RO	1 = Jabber 0 = No jabber
		HW Rst	0	
		SW Rst	Retain	

4.1.10 Interrupt Enable Register

Offset: 0x12

Bit	Name	Type		Description
15	Auto-Negotiation Error Interrupt Enable	Mode	R/W	1 = Interrupt enable 0 = Interrupt disable
		HW Rst	0	
		SW Rst	Retain	
14	Speed Changed Interrupt Enable	Mode	R/W	1 = Interrupt enable 0 = Interrupt disable
		HW Rst	0	
		SW Rst	Retain	
13	Duplex Changed Interrupt Enable	Mode	R/W	1 = Interrupt enable 0 = Interrupt disable
		HW Rst	0	
		SW Rst	Retain	
12	Page Received Interrrupt Enable	Mode	R/W	1 = Interrupt enable 0 = Interrupt disable
		HW Rst	0	
		SW Rst	Retain	
11	Link Fail Interrupt Enable	Mode	R/W	1 = Interrupt enable 0 = Interrupt disable
		HW Rst	0	
		SW Rst	Retain	
10	Link Success Interrupt Enable	Mode	R/W	1 = Interrupt enable 0 = Interrupt disable
		HW Rst	0	
		SW Rst	Retain	
9	RES	Mode	R/W	Reserved
		HW Rst	0	
		SW Rst	Retain	
8	RES	Mode	R/W	Reserved
		HW Rst	0	
		SW Rst	0	

Bit	Name	Type		Description
7	RES	Mode	R/W	Reserved
		HW Rst	0	
		SW Rst	Retain	
6	MDI Crossover Changed Interrupt Enable	Mode	R/W	1 = Interrupt enable 0 = Interrupt disable
		HW Rst	0	
		SW Rst	Retain	
5	Wirespeed-downgrade Interrupt Enable	Mode	R/W	1 = Interrupt enable 0 = Interrupt disable
		HW Rst	0	
		SW Rst	Retain	
4:2	RES	Mode	R/W	Reserved
		HW Rst	000	
		SW Rst	Retain	
1	Polarity Changed Interrupt Enable	Mode	R/W	1 = Interrupt enable 0 = Interrupt disable
		HW Rst	0	
		SW Rst	Retain	
0	Jabber Interrupt Enable	Mode	R/W	1 = Interrupt enable 0 = Interrupt disable
		HW Rst		
		SW Rst		

4.1.11 *Interrupt Status Register*

Offset: 0x13

Bit	Name	Type		Description
15	Auto-Negotiation Error	Mode	RO, LH	An error is said to occur if MASTER/SLAVE does not resolve, parallel detect fault, no common HCD, or link does not come up after negotiation is completed. 1 = Auto-Negotiation Error 0 = No Auto-Negotiation Error
		HW Rst	0	
		SW Rst	Retain	

Bit	Name	Type		Description
14	Speed Changed	Mode	RO, LH	1 = Speed changed 0 = Speed not changed
		HW Rst	0	
		SW Rst	Retain	
13	Duplex Changed	Mode	RO, LH	1 = Duplex changed 0 = Duplex not changed
		HW Rst	0	
		SW Rst	Retain	
12	Page Received	Mode	RO, LH	1 = Page received 0 = Page not received
		HW Rst	0	
		SW Rst	Retain	
11	Link Fail Interrupt	Mode	RO, LH	1 = Link down happened. 0 = Link down not happened.
		HW Rst	0	
		SW Rst	Retain	
10	Link Success Interrupt	Mode	RO, LH	1 = Link down happened. 0 = Link down not happened.
		HW Rst	0	
		SW Rst	Retain	
9	RES	Mode	RO, LH	Reserved
		HW Rst	0	
		SW Rst	Retain	
8	RES	Mode	RO	Reserved
		HW Rst	0	
		SW Rst	0	
7	RES	Mode	RO	Reserved
		HW Rst	0	
		SW Rst	0	
6	MDI Crossover Changed	Mode	RO, LH	1 = Crossover changed 0 = Crossover not changed
		HW Rst	0	
		SW Rst	Retain	

Bit	Name	Type		Description
5	Wirespeed-downgrade Interrupt	Mode	RO, LH	1 = Wirespeed-downgrade detected. 0 = No Wirespeed-downgrade.
		HW Rst	0	
		SW Rst	Retain	
4:2	RES	Mode	RO	Reserved
		HW Rst	000	
		SW Rst	000	
1	Polarity Changed	Mode	RO, LH	1 = Polarity Changed 0 = Polarity not changed
		HW Rst	0	
		SW Rst	Retain	
0	Jabber	Mode	RO, LH	1 = Jabber 0 = No jabber
		HW Rst	0	
		SW Rst	Retain	

4.1.12 Smart Speed Register

Offset: 0x14

Bit	Name	Type		Description
15:11	RES	Mode	RO	Reserved. Must be 00000000.
		HW Rst	0	
		SW Rst	0	
10:9	Reserved	Mode	R/W	Reserved
		HW Rst	2'b00	
		SW Rst	Retain	
8	RES	Mode	RO	Reserved
		HW Rst	1'b0	
		SW Rst	Update	

Bit	Name	Type		Description
7:6	RES	Mode	R/W	Reserved
		HW Rst	0	
		SW Rst	Update	
5	Smartspeed_en	Mode	R/W	The default value is one; if this bit is set to one and cable inhibits completion of the training phase, then After a few failed attempts, the Atheros card automatically downgrades the highest ability to the next lower speed: from 100 to 10.
		HW Rst	1	
		SW Rst	Update	
4:2	Smartspeed_retry_limit	Mode	R/W	The default value is three; if these bits are set to three, then the Atheros card will attempt five times before downgrading; The number of attempts can be changed through setting these bits.
		HW Rst	3'b011	
		SW Rst	Update	
1	Bypass_smartspeed_timer	Mode	R/W	The default value is zero; if this bit is set to one, the Smartspeed FSM will bypass the timer used for stability.
		HW Rst	0	
		SW Rst	Update	
0	RES	Mode	R/W	Reserved.
		HW Rst	0	
		SW Rst	0	

4.1.13 Receive Error Count Register

Offset: 0x15

Bit	Name	Type		Description
15:0	Receive Error Count	Mode	RO	Counter will peg at 0xFFFF and will not roll over. (when rx_dv is valid, count rx_er numbers) (in this version, only for 100Base-T)
		HW Rst	0	
		SW Rst	0	

4.1.14 Virtual Cable Tester Control Register

Offset: 0x16

Bit	Name	Type		Description
15:11	Vct_dbg_psw	Mode	RO	For VCT debug
		HW Rst	0	
		SW Rst	0	
10	vct_wp_ Max_vcode[3]	Mode	RO	For VCT debug
		HW Rst	1'b1	
		SW Rst	Retain	
9:8	MDI Pair Select	Mode	R/W	Virtual Cable Tester™ Control registers. Use the Virtual Cable Tester Control Registers to select which MDI pair is shown in the Virtual Cable Tester Status register. 00 = MDI[0] pair 01 = MDI[1] pair 10 = Reserved 11 = Reserved
		HW Rst	00	
		SW Rst	00	
7:5	vct_wp_ Max_vcode[2:0]	Mode	RO	For VCT debug
		HW Rst	3'b111	
		SW Rst	Retain	
4:1	vct_np_ Max_vcode[3:0]	Mode	R/W	For VCT debug
		HW Rst	3'b100	
		SW Rst	Retain	

Bit	Name	Type		Description
0	Enable Test	Mode	R/W	When set, hardware automatically disable this bit when VCT is done. 1 = Enable VCT Test 0 = Disable VCT Test
		HW Rst	0	
		SW Rst	Retain	

4.1.15 LED Control Register

Offset: 0x18

Bit	Name	Type		Description
15	Disable LED	Mode	R/W	Control the output LED pins. 0 = Enable 1 = Disable
		HW Rst	0	
		SW Rst	Retain	
14:12	LED On Time	Mode	R/W	000 = 5 ms 001 = 10ms 010 = 21 ms 011 = 42ms 100 = 84 ms 101 = 168ms 110 to 111 = 42ms
		HW Rst	3'b011	
		SW Rst	Retain	
11	Force Interrupt	Mode	RO	Always 0
		HW Rst	0	
		SW Rst	0	
10:8	LED Off Time	Mode	R/W	000 = 21 ms 001 = 42 ms 010 = 84 ms 011 =168 ms 100 =330 ms 101 = 670 ms 110 to 111 = 168ms
		HW Rst	3'b010	
		SW Rst	0	
7:5	RES	Mode	RO	Reserved
		HW Rst	000	
		SW Rst	000	
4:3	LED_LINK Control	Mode	R/W	00 = Direct LED mode 11 = Master/Slave LED mode 01, 10 = Combined LED modes
		HW Rst	0	
		SW Rst	Retain	

Bit	Name	Type		Description
2	RES	Mode	R/W	Reserved
		HW Rst	0	
		SW Rst	Retain	
1	RES	Mode	R/W	Reserved
		HW Rst	0	
		SW Rst	Retain	
0	RES	Mode	R/W	Reserved
		HW Rst	0	
		SW Rst	Retain	

4.1.16 Virtual Cable Tester Status Register

Offset: 0x1C

Bit	Name	Type		Description
15:10	RES	Mode	RO	Reserved
		HW Rst	0	
		SW Rst	0	
9:8	Status	Mode	RO	The content of the Virtual Cable Tester Status Registers applies to the cable pair selected in the Virtual Cable Tester™ Control Registers. 11 = Link-up state, no short or open in cable 00 = Valid test, normal cable (no short or open in cable) 10 = Valid test, open in cable (Impedance > 333 ohms) 01 = Valid test, short in cable (Impedance < 33 ohms)
		HW Rst	00	
		SW Rst	00	
7:0	Delta_Time	Mode	R/W	Delta time indicates distance along the cable
		HW Rst	0	
		SW Rst	0	

4.1.17 Debug Port (Address Offset Set) Register

Offset: 0x1D

Bit	Name	Type		Description
15:6	RES	Mode	RO	Reserved
		HW Rst	0	
		SW Rst	0	
5:0	Addres Offset	Mode	R/W	The address index of the register will be written or read.
		HW Rst	0	
		SW Rst	0	

4.1.18 Debug Port 2 (R/W Port) Register

Offset: 0x1E

Bit	Name	Type		Description
15:0	Debug Data Port	Mode	R/W	The data port for the debug register. Before accessing this register, you must set the address offset first.
		HW Rst	0x02EE	
		SW Rst	0x02EE	

4.2 Power Saving and Debug Register Summary

Table 4-3. **Register Summary**

Offset	Register	Page
0x12	Test Configuration for 10Base-T	page 44
0x10	Test Configuration for 100Base-Tx	page 45
0x0B	Hibernate Control	page 47
0x29	Power Saving Control	page 48

4.2.19 10Base-T Test Configuration Register

Offset: 0x12

Bit	Name	Type		Description
15:14	Interval_sel_timer	Mode	R/W	Controls the interval that PHY detects whether the data frames on the cable are MLT-3 coded. This logic is used to divide Manchester code from MLT-3 code.
		HW Rst	01	
		SW Rst	Retain	
13:12	Triger_sel_timer	Mode	R/W	Controls the threshold that PHY detects at the end of the interval whether the data frames on the cable are MLT-3 coded. This logic is used to divide Manchester code from MLT-3 code.
		HW Rst	00	
		SW Rst	Retain	
11	En_mask_bt	Mode	R/W	1: enable the function of dividing Manchester code from MLT-3 code. 0: disable the function.
		HW Rst	1	
		SW Rst	0	
10	En_10bt_idle	Mode	R/W	1: In 10BT mode , if there's no data or NLP to transmit, shut off dac; otherwise turn on the dac; 0: In 10BT, dac will not be turn off.
		HW Rst	1	
		SW Rst	0	
9:6	RES	Mode	RO	Reserved
		HW Rst	1000	
		SW Rst	1000	
5	Test_mode[2]	Mode	R/W	bit 2 of test_mode
		HW Rst	0	
		SW Rst	0	

Bit	Name	Type		Description
4	En_longcable	Mode	R/W	Enable long cable test
		HW Rst	0	
		SW Rst	Retain	
3	RES	Mode	R/W	Reserved
		HW Rst	0	
		SW Rst	Retain	
2	Loopback mode select	Mode	RO	1: lpbk2-deep in Loopback mode 0: lpbk1-shallow in Loopback mode (connect to dig10.test_mode_i[0])
		HW Rst	1	
		SW Rst	1	
1:0	Test_mode[1:0]	Mode	R/W	[001]: packet with all ones, 10MHz sine wave, For harmonic test. [010]: pseudo random, for TP_IDLE/Jitter/Differential Voltage test. [011]: normal link pulse only, [100]: 5MHz sin wave. Others: normal mode.
		HW Rst	0	
		SW Rst	0	

4.2.20 100Base-TX Test Configuration Register

Offset: 0x10

Bit	Name	Type		Description
15	RES	Mode	R/W	Reserved
		HW Rst	0	
		SW Rst	Retain	
14:8	RES	Mode	R/W	Reserved
		HW Rst	0111001	
		SW Rst	Retain	
7	Jitter_test	Mode	R/W	100Base-Tx Jitter test
		HW Rst	0	
		SW Rst	Retain	

Bit	Name	Type		Description
6	Os_test	Mode	R/W	100Base-Tx Overshoot test
		HW Rst	0	
		SW Rst	Retain	
5	Dcd_test	Mode	R/W	100Base-Tx DCD test
		HW Rst	0	
		SW Rst	Retain	
4	RES	Mode	R/W	Reserved
		HW Rst	0	
		SW Rst	0	
3	RES	Mode	R/W	Reserved
		HW Rst	0	
		SW Rst	0	
2	RES	Mode	R/W	Reserved
		HW Rst	0	
		SW Rst	0	
1	RES	Mode	R/W	Reserved
		HW Rst	0	
		SW Rst	0	
0	RES	Mode	R/W	Reserved
		HW Rst	0	
		SW Rst	0	

4.2.21 Hibernate Control Register

Offset: 0x0B

Bit	Name	Type		Description
15	Ps_hib_en	Mode	RO	Power hibernate conrol bit; '1' : hibernate enable '0' : hibernate disable
		HW Rst	1	
		SW Rst	0	
14	RES	Mode	RO	Reserved
		HW Rst	0	
		SW Rst	0	
13	RES	Mode	RO	Reserved
		HW Rst	1	
		SW Rst	1	
12	RES	Mode	RO	Reserved
		HW Rst	1	
		SW Rst	1	
11	RES	Mode	RO	Reserved
		HW Rst	1	
		SW Rst	1	
10	RES	Mode	RO	Reserved
		HW Rst	1	
		SW Rst	1	
9:0	RES	Mode	RO	Reserved
		HW Rst	0	
		SW Rst	0	

4.2.22 Power Saving Control

Offset: 0x29

Bit	Name	Type		Description
15	TOP_PS_EN	Mode	RO	'1' : Top level Power Saving Enable '0' : Top level Power Saving Disable
		HW Rst	1	
		SW Rst	Retain	
14:12	RES	Mode	R/W	Reserved
		HW Rst	3'h3	
		SW Rst	Retain	
11:9	Dac_amp_100	Mode	R/W	Control amplitude of transmit signal in 100BT mode. 000: -2% …… 111: +12%
		HW Rst	3'h3	
		SW Rst	Retain	
8:6	Dac_amp_10	Mode	R/W	Control amplitude of transmit signal in 10BT mode. 000: -2% …… 111: +12%
		HW Rst	3'h3	
		SW Rst	Retain	
5:1	RES	Mode	R/W	Reserved
		HW Rst	10010	
		SW Rst	10010	
0	RES	Mode	R/W	Reserved
		HW Rst	1	
		SW Rst	Retain	

5. Package Dimensions

The AR8032 is packaged in a QFN 32. The body size is 5 mm by 5 mm. The package drawings and dimensions are provided in Figure 5-1 and Table 5-1.

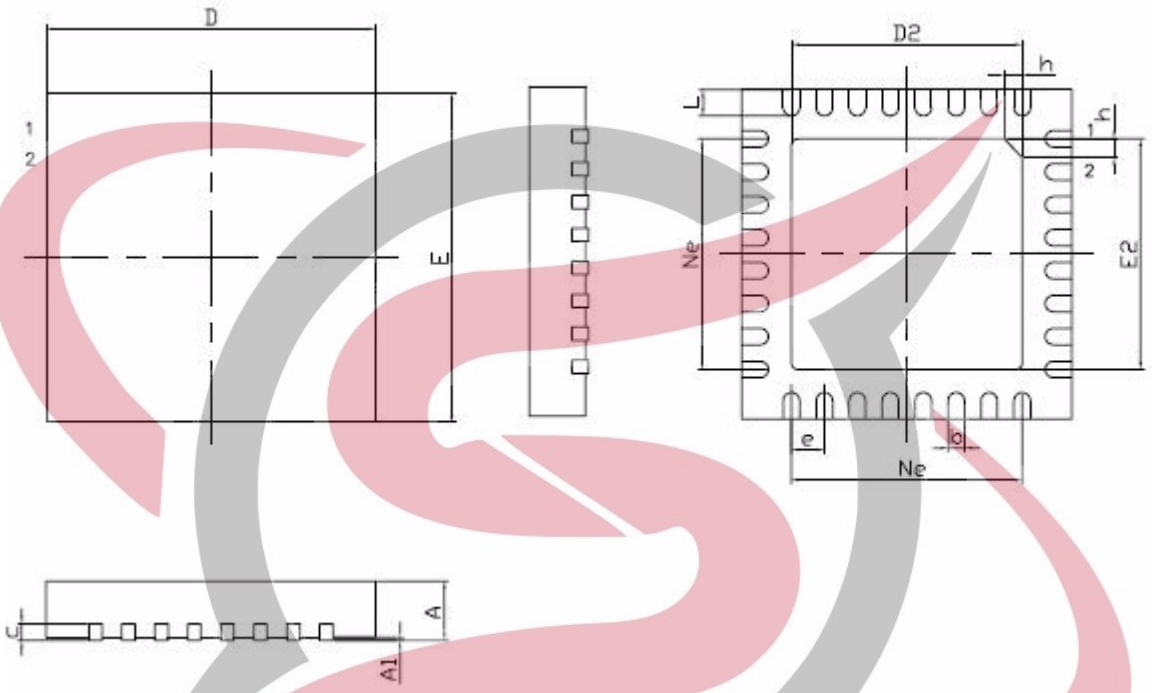

Figure 5-1. **Package Views**

Table 5-1. **Package Dimensions**

Dimension Label	Min	Nom	Max	Unit
A	0.70	0.75	0.80	mm
A1	—	0.01	0.05	mm
b	0.18	0.25	0.30	mm
c	0.18	0.20	0.25	mm
D	4.90	5.00	5.10	mm
D2		3.50REF		mm
e		0.50 Basic		mm
Ne		3.50 Basic		mm
E	4.90	5.00	5.10	mm
E2		3.50REF		mm
L	0.35	0.40	0.45	mm
h	0.30	0.35	0.40	mm

Notes:

1. Dimensioning and tolerences conform to JEDEC MO-220

6. Ordering Information

The order number AR8032-BL1A specifies a Commercial version of the AR8032.

The order number AR8032-BL1B specifies an Industrial version of the AR8032.

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